

DIGITALLY PROGRAMMABLE MULTI-SCROLL CHAOS GENERATOR ON FPGA

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Multi-scroll chaotic attractors exhibit higher unpredictability than double-scroll attractors. However, the more number of scrolls cost the more usage of sources. To overcome this problem, the attractor design should be simplified. This paper presents a systematic approach that enables to realize digital piece wise linear (PWL) function in nonlinear dynamical system and to obtain whole behaviors in only one model. The proposed design requires only number of scroll as input and can realize chaotic PWL signal with a fewer number of FPGA resources. In the implementation stage of the study, the discrete mathematical equations of the chaotic attractor is modelled in Xilinx System Generator (XSG) platform and realized by using Xilinx Kintex-7 KC705 Evaluation Board.

Key words: *chaos, discrete time, multi-scroll, xilinx system generator.*

1. Introduction

Chaotic systems are complex, irregular and nonlinear dynamical systems that can cause to extraordinary differences in the system behavior [1]. The dynamics of the chaotic systems have attracted attention of many researchers and there are several studies on it. In 1963, Edward Lorenz describes the motion of a fluid under the conditions of Rayleigh-Benard flow [2,3] and it has become a paradigm [4]. The system consists of many features of the chaotic dynamics.

The simplest chaotic circuit is well known Chua's circuit that has piece wise linear (PWL) resistor [5, 6] which is the only nonlinear element in the circuit. The Chua's circuit has become a standard due to its simplicity and universality [7]. In recent years, there are several studies using Chua's circuit in the area of chaos control [8-12] and synchronization [13-15]. The most important advantages of the circuit are that it can be build passive circuit elements easily and the chaos in the circuit can be proved mathematically.

The generalized Chua's circuit has only one nonlinear circuit component that is nonlinear resistor. In [16], it is shown that by modifying the nonlinear resistor, the Chua's circuit can generate more complex behavior. By introducing additional breakpoints for nonlinear resistor, multi-scroll (n-scroll) chaotic attractor is proposed in [17, 6]. After experimental confirmation of multi-scroll attractors referred to the Chua's circuit, multi-scroll chaotic attractors have been studied and different approaches have been proposed [18-21].

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In this study, a systematic approach that enables to realize digital piece wise linear (PWL) function in the Chua's circuit model and to obtain whole behaviors in only one model. The proposed multi-scroll chaotic attractors design requires only number of scroll as input and can realize chaotic PWL signal with a fewer number of FPGA resources. In the implementation stage of the study, the discrete mathematical equations of the chaotic system is modelled in Xilinx System Generator (XSG) platform and realized by using Xilinx Kintex-7 KC705 Evaluation Board.

Herewith this introduction, in Section 2, the Chua's circuit is described and MATLAB-Simulink model is executed and chaotic behavior of the multi-scroll chaotic attractors are obtained. Section 3 includes the discretization method, Xilinx System Generator designs and realization of the system. At the end, Section 4 concludes the paper.

2. The Chua's Circuit

The Chua's circuit is the simplest electronic chaotic circuit that has only one nonlinear component called nonlinear resistor. The circuit diagram is shown in Fig. 1 and can be described by the following set of dynamical equations as proposed in [5, 6];

$$\begin{aligned} \dot{I}_L(t) &= (-1/L) V_2 \\ \dot{V}_2(t) &= (1/C_2) I_L - (1/RC_2)(V_2 - V_1) \\ \dot{V}_1(t) &= (1/RC_1)(V_2 - V_1) - (1/C_1)f(V_1) \end{aligned} \quad (1)$$

$$\begin{aligned} f_e(V_1) &= m_{2n-1}V_1 + \frac{1}{2} \sum_{i=1}^{2n-1} (m_{i-1} - m_i)(|V_1 + b_i| - |V_1 - b_i|) \\ f_o(V_1) &= m_{2n-1}V_1 + \frac{1}{2} \sum_{i=2}^{2n-1} (m_{i-1} - m_i)(|V_1 + b_i| - |V_1 - b_i|) \end{aligned} \quad (2)$$

where I_L , V_2 , V_1 , m_i and b_i stand for current of inductor, the voltages across C_2 and C_1 , the slope of the i -th segment and the breakpoints of the nonlinear resistor, respectively [17]. The nonlinear PWL function is represented as $f(\cdot)$ and has two components $f_e(\cdot)$ and $f_o(\cdot)$ that are the function for the case of even and odd number of scrolls respectively. Therefore, the system can change its behavior regarding to number of scrolls. Furthermore, the system parameters are given as $m_0 = -3.2$ ms, $m_1 = m_3 = m_5 = m_7 = m_9 = -0.2$ ms, $m_2 = m_4 = m_6 = m_8 = -2.2$ ms, $C_1 = 10$ nF, $C_2 = 100$ nF and $L = 18.68$ mH.

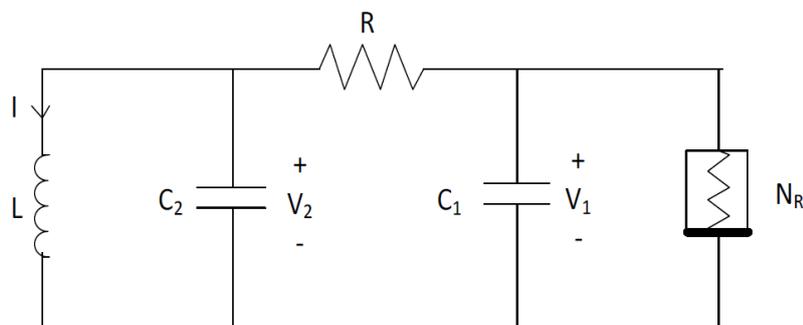


Figure 1: Dynamical Chua's circuit.

The multi-scroll chaotic attractors are obtained according to the number of scrolls, the breakpoint voltages and resistor values. Table 1 shows the value of resistor and the breakpoint voltages in contrast to number of scrolls.

Table 1: Determined variable system parameters in contrast to number of scrolls [6]

System parameters	Number of scrolls					
	5	6	7	8	9	10
R(Ω)	1515	1572	1515	1552	1381	1381
b ₁ (V)	-	0.1	-	0.1	-	0.1
b ₂ (V)	0.8	1.1	0.8	1.1	0.8	1.1
b ₃ (V)	1.4	1.55	1.4	1.55	1.4	1.55
b ₄ (V)	3.2	3.2	3.2	3.2	3.2	3.2
b ₅ (V)	3.9	3.85	3.9	3.85	3.9	3.85
b ₆ (V)	-	-	5.8	5.84	5.8	5.84
b ₇ (V)	-	-	6.4	6.6	6.4	6.6
b ₈ (V)	-	-	-	-	8.3	8.7
b ₉ (V)	-	-	-	-	9.2	9.45

The differential equations of the system can be simulated on MATLAB Simulink platform to observe system behavior in contrast to number of scrolls [22, 23]. The MATLAB Simulink model has three sub blocks that are tank resonator, PWL and control blocks. The tank resonator block consists of dynamical Chua's circuit equations except for PWL function $f(\cdot)$. The control unit decides which output of PWL block to transmit to the tank resonator according to the scroll value applied to the control unit input.

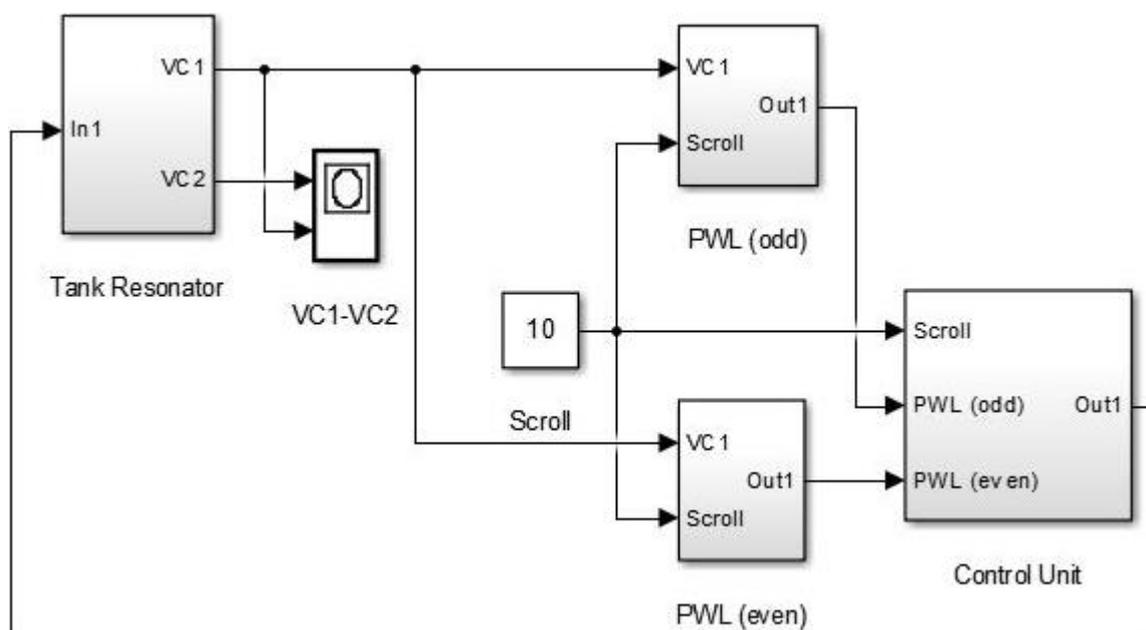


Figure 2: MATLAB Simulink model of the multi-scroll attractor.

The system behaviors for 9 and 10 scrolls are obtained regarding to system parameters given in Fig. 3. Before execution of Simulink model given in Fig. 2, the values of resistor and scroll must be typed in MATLAB command window as given in Table 1.

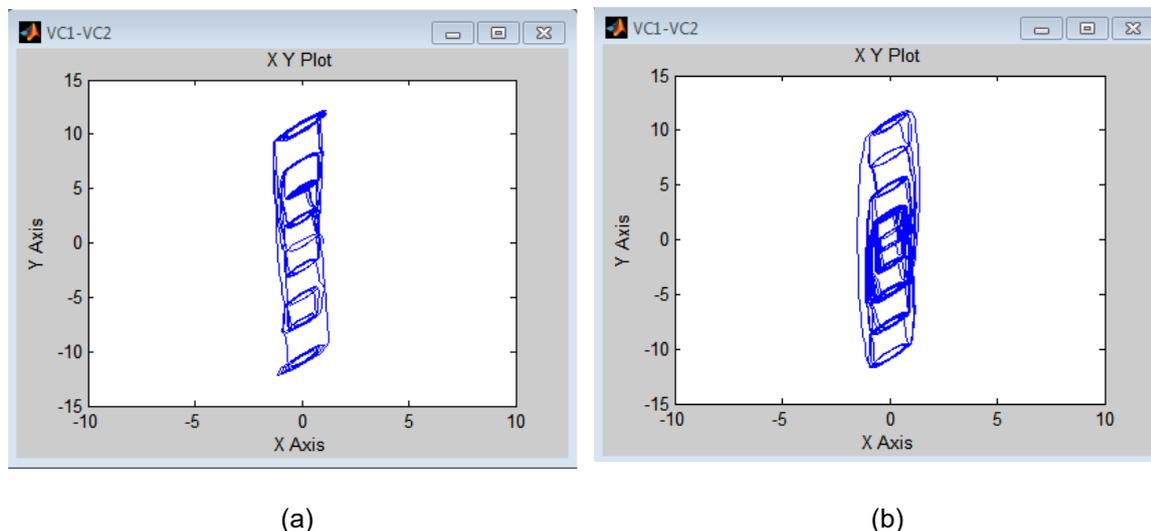


Figure 3: Phase plane portraits of $V_{C1} - V_{C2}$ for (a) 9-scroll and (b) 10-scroll.

3. Multi-scroll Attractor Design on FPGA

3.1. Discretization of differential equations

In digital applications, researchers use discrete time modelling in order to embed the system to embedded systems such as microprocessors, FPGA, ARM and so on. There are three types of discretization methods that are Taylor series expansion, Runge-Kutta and Euler integration methods [24]. In this study, Forward Euler integration method is used to discretize the dynamical Chua's circuit equations.

The expression of FE method is given in Eq. 3 and discretized model is expressed in Eq. 4 and 5 with the time step h ;

$$\begin{aligned} \dot{x}(t) &= \frac{x(t+h) - x(t)}{h} \\ \dot{y}(t) &= \frac{y(t+h) - y(t)}{h} \\ \dot{z}(t) &= \frac{z(t+h) - z(t)}{h} \end{aligned} \quad (3)$$

$$\begin{aligned} x[n+1] &= x[n] - \frac{h}{L}y[n] \\ y[n+1] &= y[n] + h \left(\frac{1}{C_2}x[n] - \frac{1}{RC_2}(y[n] - z[n]) \right) \\ z[n+1] &= z[n] + h \left(\frac{1}{RC_1}(y[n] - z[n]) - \frac{1}{C_1}f(z[n]) \right) \end{aligned} \quad (4)$$

$$f_e(z[n]) = m_{2n-1}y[n] + \frac{1}{2} \sum_{i=1}^{2n-1} (m_{i-1} - m_i)(|y[n] + b_i| - |y[n] - b_i|)$$

$$f_o(z[n]) = m_{2n-1}y[n] + \frac{1}{2} \sum_{i=2}^{2n-1} (m_{i-1} - m_i)(|y[n] + b_i| - |y[n] - b_i|)$$
(5)

where x, y, z denote I_L, V_2 and V_1 respectively. The discrete model of any system can be realized on FPGA after design both programming Verilog or VHDL languages and Xilinx System Generator (XSG) / Model Composer easily. In this study, XSG platform is used to realize the model. The Xilinx System Generator technology is a high level MATLAB-Simulink based software platform. In that platform, designs can be created easily to execute Hardware Co-Simulation and implement real-time FPGA applications [25].

3.2. Design and realization

In the design stage, discretized equations of chaotic Chua’s circuit is modelled on XSG platform by using standard XSG arithmetic blocks. XSG blocks use fixed-point number format. Therefore, 32-bit signed fractional numbers are used in arithmetic operations such as addition and multiplication process of the design. $Qm.n$ is used for representing fixed-point number format where m indicates the number of bits that are arranged for integer part of number while n for fractional part. Therefore, the format is arranged as $Q16.16$ to get resolution as $2^{-n} = 2^{-16} = 1.5259 \text{ e-}5$. Fig. 4, 5, 6 and 7 illustrate the XSG design of the discretized tank resonator, control unit, PWL (even) and subsystem of the PWL (even), respectively.

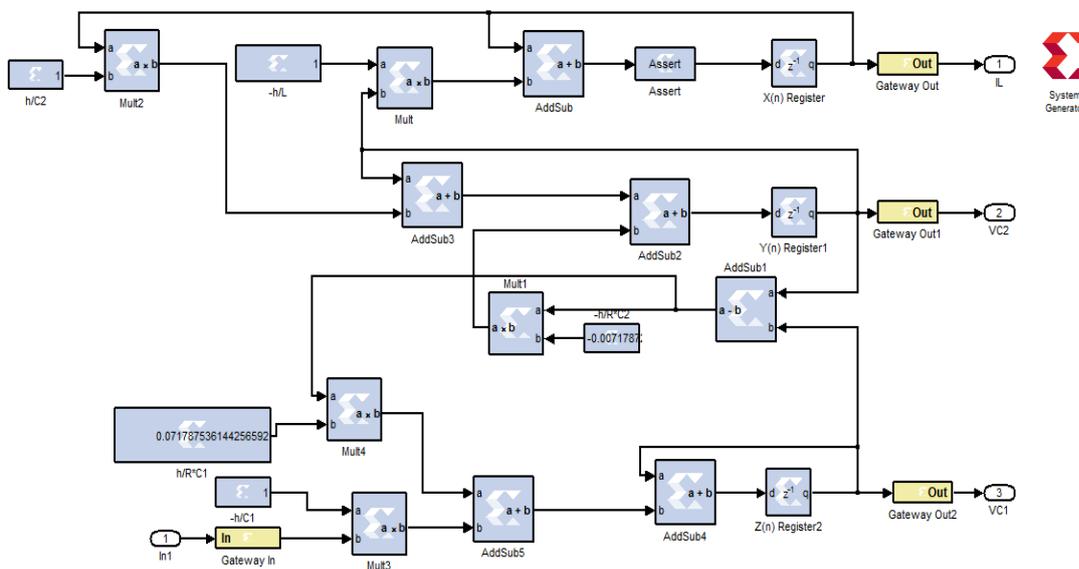


Figure 4: XSG design of tank resonator.

The tank resonator XSG design requires only one input that is one of the PWL function (odd or even). The whole design is constructed with adder, multiplier, constant, multiplexer, slice, gateway in/out, input/output, register and absolute value blocks. The initial conditions of state variables are given as $(I_L, V_2, V_1) = (0, 0, 0.01)$.

The control unit determines whether the value of scroll is even or odd using multiplexer. If the value of the scroll is even, output value of PWL (even) block is transmitted to tank resonator input or vice versa in each iteration.

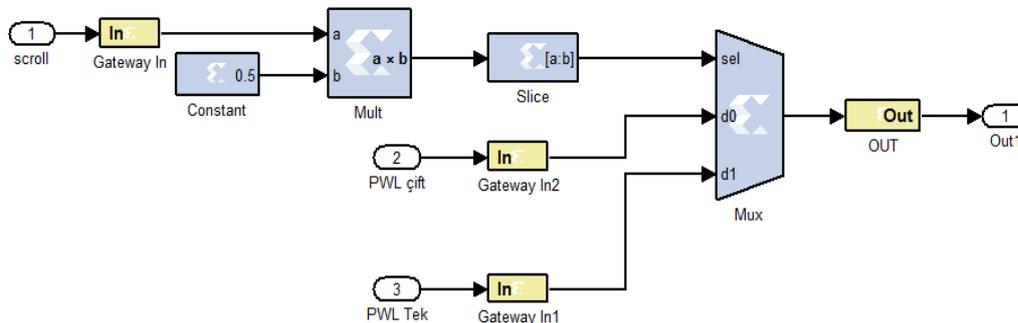


Figure 5: XSG design of the control unit.

In the Fig. 8, chaotic attractor behaviours for 9 and 10 scrolls are obtained regarding to system parameters by executing XSG simulation. In the implementation stage of study, Xilinx Kintex-7 Evaluation Board is connected to the host computer via JTAG cable to obtain hardware based co-simulation process.

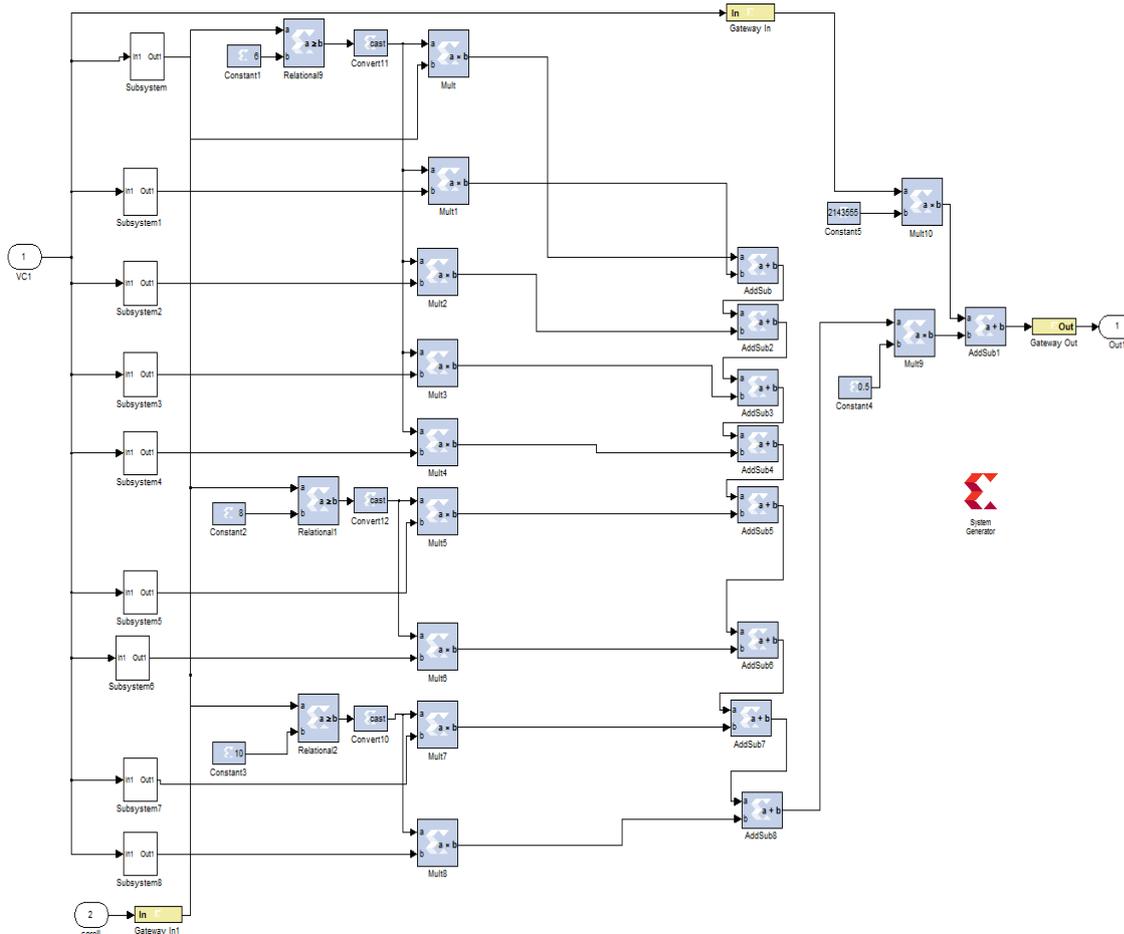


Figure 6: XSG design of PWL (even).

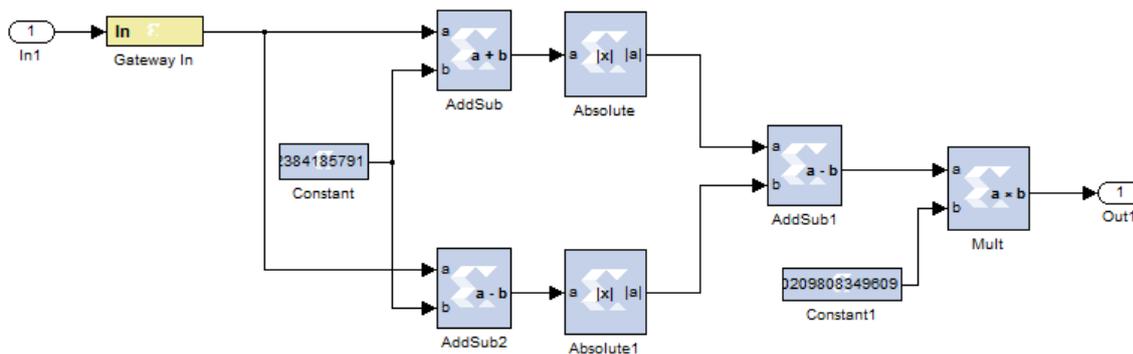


Figure 7: XSG design of subsystem of the PWL (even).

Hardware Co-simulation process is executed on selected FPGA board to determine whether the design can be realized or not. Whole parts of design is merged to one design file and it is shown in Fig. 9. For an example of study, the multi-scroll attractor design is co-simulated and realized for 5-scroll and the design is given in Fig. 10. As it can be seen that JTAG Hardware Co-simulation block is also added to design. As a result of this study, Fig. 11 shows realization of the chaotic attractor for 5-scroll.

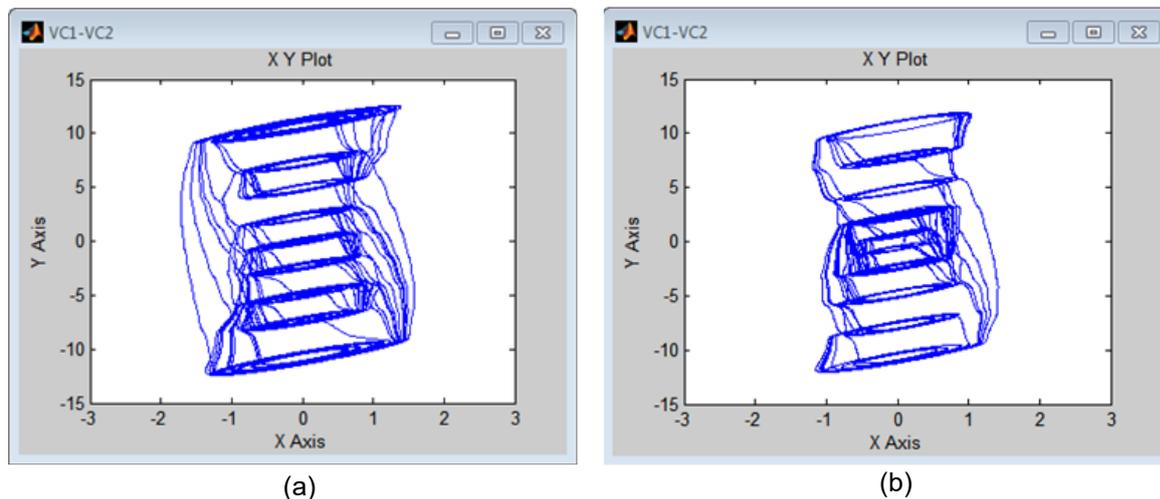


Figure 8: XSG simulation result for phase plane portraits of $V_{C1} - V_{C2}$ for (a) 9-scroll and (b) 10-scroll.

The multi-scroll chaotic attractor is realized in XSG JTAG Hardware Co-simulation platform and Table 2 shows the resource utilization of the attractor for 5-scroll.

Table 2. Resource utilization of 5-scroll chaotic attractor on FPGA chip

FPGA Resources	Usage
Flip-Flops	486
Logic Slices	1467
IOB	4

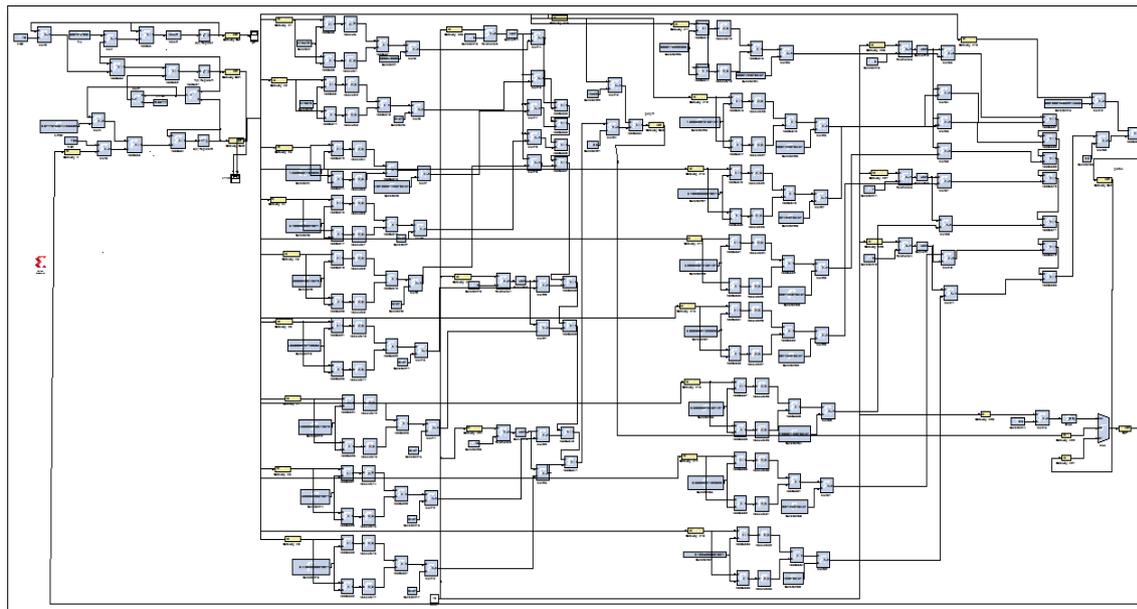


Figure 9: The whole design merged to one design file.

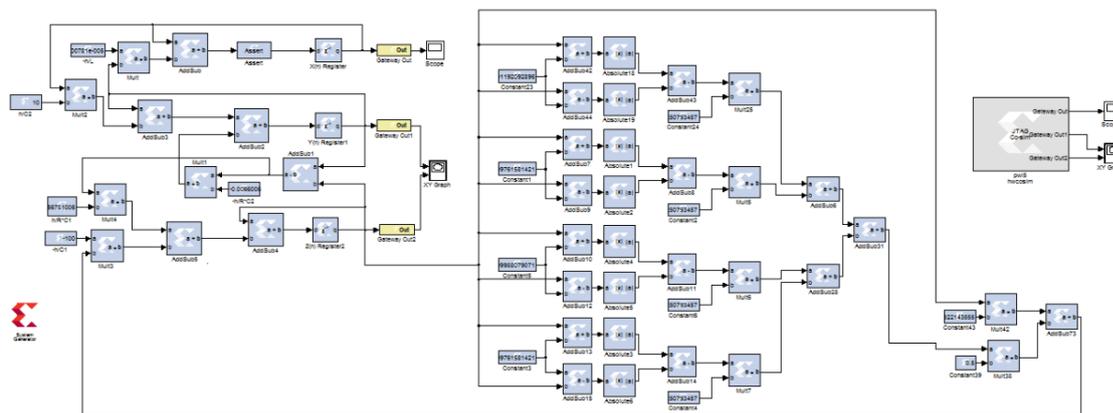


Figure 10: XSG JTAG Hardware Co-simulation design for 5-scroll.

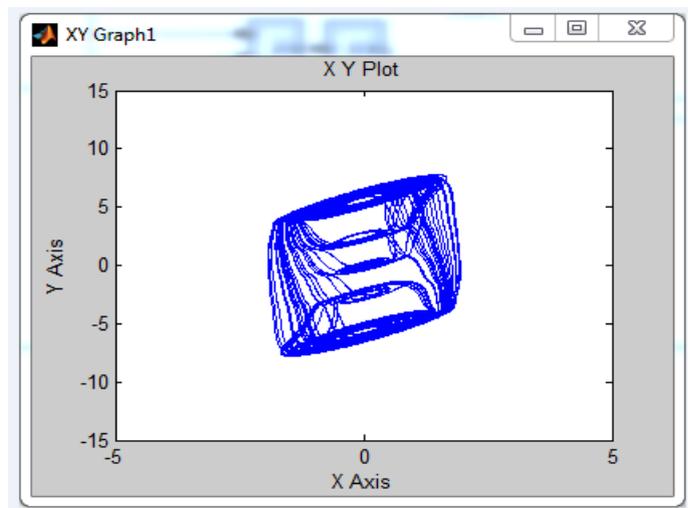


Figure 11: XSG JTAG Hardware Co-simulation result, phase plane portrait of $V_{C1} - V_{C2}$ for 5-scroll.

4. Conclusions

In this study, the chaotic Chua's circuit is simulated in MATLAB, discretized using Forward Euler discretization method and modelled on XSG platform. The advantages of our study are that the design is realized on FPGA with fewer number of resource, requires only the number of scroll as input and is fully programmable. Therefore, the design can be easily adapted to secure communication and synchronization circuits.

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